CLAIMS

What is claimed is:

1. A method of testing reliability in an integrated circuit (IC) including an array of test circuits, each test circuit including a resistor, the method comprising:

selecting a first test circuit from the array of test circuits, the first test circuit comprising a first current path traversing a first resistor in the first test circuit;

measuring, after selecting the first test circuit, a first pre-stress resistance value for the first resistor;

applying, after measuring the first pre-stress resistance value, a first high stress current through the first current path;

removing the first high stress current from the first current path; and

measuring, after removing the first high stress current, a first post-stress resistance value for the first resistor.

2. The method of Claim 1, further comprising de-selecting the first test circuit after measuring the first post-stress resistance value.

3. The method of Claim 1, further comprising:

de-selecting the first test circuit;

selecting a second test circuit from the array of test circuits, the second test circuit comprising a second current path traversing a second resistor in the second test circuit;

measuring, after selecting the second test circuit, a second pre-stress resistance value for the second resistor;

de-selecting the second test circuit; and

re-selecting the first test circuit.

4. The method of Claim 3, wherein de-selecting the first test circuit, selecting the second test circuit, measuring the second pre-stress resistance value, de-selecting the second test circuit, and re-selecting the first test circuit occur after measuring the first pre-stress resistance value and before applying the first high stress current.

5. The method of Claim 3, further comprising:

de-selecting the first test circuit;

re-selecting the second test circuit;

applying a second high stress current through the second current path;

removing the second high stress current from the second current path;

de-selecting the second test circuit; and

re-selecting the first test circuit.

6. The method of Claim 5, wherein de-selecting the first test circuit, re-selecting the second test circuit, applying the second high stress current, removing the second high stress current, de-selecting the second test circuit, and re-selecting the first test circuit occur after removing the first high stress current from the first current path and before measuring the first post-stress resistance value for the first resistor.

7. The method of Claim 5, further comprising, after measuring the first post-stress resistance value for the first resistor:

de-selecting the first test circuit;

re-selecting the second test circuit; and

measuring a second post-stress resistance value for the second resistor.

8. The method of Claim 7, wherein de-selecting the first test circuit, re-selecting the second test circuit, and measuring the second post-stress resistance value occur after measuring the first post-stress resistance value.

9. The method of Claim 1, wherein:

selecting the first test circuit comprises:

selecting a first row and a first column from the array, the first test circuit being in the first row and the first column,

enabling the first current path through the first test circuit, and

providing access to first and second terminals of the first resistor; and

deselecting the first test circuit comprises:

disabling the first current path through the first test circuit, and

removing access to the first and second terminals of the first resistor.

10. The method of Claim 1, wherein:

measuring the first pre-stress resistance value for the first resistor comprises applying a first non-stressing current through the first current path and measuring a first voltage differential between the first and second terminals of the first resistor; and

measuring the first post-stress resistance value for the first resistor comprises applying a second non-stressing current through the first current path and measuring a second voltage differential between the first and second terminals of the first resistor.

11. The method of Claim 1, wherein each test circuit further includes a short testing structure, the method further comprising:

testing, before applying the first high stress current, for a pre-stress short between the first resistor and the short testing structure; and

testing, after applying the first high stress current, for a post-stress short between the first resistor and the short testing structure.

12. The method of Claim 11, wherein each of testing for the pre-stress short and testing for the post-stress short comprises:

applying a positive voltage level at one end of the first current path; and

checking for the positive voltage level on the short testing structure.